



National Institute of Technology Raipur

G.E. Road, Raipur Chhattisgarh - 492010, India

Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : ABHIRAM KUMAR
Mother's Name : SAROJ DEVI
Father's Name : DWARIKA PRASAD

Roll No : 19266001

Semester : II
Enrollment No : 190075

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	74	30	21	20	12	150	107	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	81	30	24	20	20	150	125	E	09	4.00
ET41213VL	VLSI System Design	100	82	30	22	20	19	150	123	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	84	30	23	20	15	150	122	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	77	30	17	20	17	150	111	A	08	4.00
ET41221VL	Analog IC Design Lab	50	34			75	55	125	89	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	44			75	68	125	112	E	09	2.00
PASS		SPI : 8.50		CPI : 8.75		Total:		1000	789		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : CHUMKI DAS
Mother's Name : ANITA DAS
Father's Name : NITYANANDA DAS

Roll No : 19266002

Semester : II
Enrollment No : 190039

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	75	30	22	20	14	150	111	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	80	30	22	20	20	150	122	E	09	4.00
ET41213VL	VLSI System Design	100	80	30	24	20	19	150	123	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	81	30	24	20	18	150	123	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	77	30	20	20	18	150	115	A	08	4.00
ET41221VL	Analog IC Design Lab	50	42			75	68	125	110	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	40			75	67	125	107	E	09	2.00
PASS		SPI : 8.66		CPI : 8.50		Total:		1000	811		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : DIKSHA AGRAWAL

Semester : II

Mother's Name : POONAM AGRAWAL

Roll No : 19266003

Enrollment No : 190053

Father's Name : PRADEEP AGRAWAL

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	74	30	24	20	18	150	116	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	80	30	24	20	20	150	124	E	09	4.00
ET41213VL	VLSI System Design	100	76	30	19	20	18	150	113	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	81	30	24	20	17	150	122	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	75	30	17	20	18	150	110	A	08	4.00
ET41221VL	Analog IC Design Lab	50	35			75	55	125	90	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	40			75	68	125	108	E	09	2.00
PASS		SPI : 8.33		CPI : 8.41		Total:		1000	783		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : G MAHESH

Semester : II

Mother's Name : G CHANDRA KALA

Roll No : 19266004

Enrollment No : 190718

Father's Name : G VENKATASWAMY

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	66	30	19	20	18	150	103	B	07	4.00
ET41212VL	System on Programmable Chip Design	100	78	30	22	20	20	150	120	E	09	4.00
ET41213VL	VLSI System Design	100	77	30	20	20	19	150	116	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	80	30	22	20	14	150	116	A	08	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	70	30	15	20	16	150	101	B	07	4.00
ET41221VL	Analog IC Design Lab	50	42			75	67	125	109	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	40			75	66	125	106	E	09	2.00
PASS		SPI : 8.00		CPI : 8.08		Total:		1000	771		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : JASOBANTA SAHOO

Semester : II

Mother's Name : MAMATA SAHOO

Roll No : 19266005

Enrollment No : 190764

Father's Name : JAYANTA KUMAR SAHOO

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	65	30	19	20	14	150	98	B	07	4.00
ET41212VL	System on Programmable Chip Design	100	73	30	17	20	20	150	110	A	08	4.00
ET41213VL	VLSI System Design	100	76	30	24	20	20	150	120	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	77	30	24	20	17	150	118	A	08	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	66	30	12	20	16	150	94	B	07	4.00
ET41221VL	Analog IC Design Lab	50	40			75	59	125	99	A	08	2.00
ET41222VL	System on Programmable chip Design Lab	50	42			75	68	125	110	E	09	2.00
PASS		SPI : 7.91		CPI : 7.87		Total:		1000	749		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : JYOTI KUMARI

Semester : II

Mother's Name : GITA DEVI

Roll No : 19266006

Enrollment No : 190048

Father's Name : VINOD KUMAR

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	72	30	24	20	16	150	112	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	51	30	20	20	20	150	91	B	07	4.00
ET41213VL	VLSI System Design	100	73	30	20	20	19	150	112	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	78	30	24	20	19	150	121	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	75	30	22	20	19	150	116	A	08	4.00
ET41221VL	Analog IC Design Lab	50	41			75	66	125	107	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	42			75	65	125	107	E	09	2.00
PASS		SPI : 8.16		CPI : 8.08		Total:		1000	766		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : JYOTI SAHU
Mother's Name : PADMANI SAHU
Father's Name : ANAND RAM SAHU

Roll No : 19266007

Semester : II
Enrollment No : 190074

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	75	30	29	20	14	150	118	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	80	30	22	20	20	150	122	E	09	4.00
ET41213VL	VLSI System Design	100	81	30	26	20	18	150	125	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	88	30	27	20	20	150	135	O	10	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	79	30	20	20	18	150	117	A	08	4.00
ET41221VL	Analog IC Design Lab	50	41			75	67	125	108	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	47			75	69	125	116	O	10	2.00
PASS		SPI : 8.91		CPI : 8.79		Total:		1000	841		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : KAJAL VERMA
Mother's Name : LEKHA VERMA
Father's Name : L.S. VERMA

Roll No : 19266008

Semester : II
Enrollment No : 190763

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	65	30	23	20	14	150	102	B	07	4.00
ET41212VL	System on Programmable Chip Design	100	78	30	22	20	20	150	120	E	09	4.00
ET41213VL	VLSI System Design	100	75	30	20	20	17	150	112	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	75	30	23	20	15	150	113	A	08	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	67	30	15	20	16	150	98	B	07	4.00
ET41221VL	Analog IC Design Lab	50	34			75	56	125	90	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	42			75	65	125	107	E	09	2.00
PASS		SPI : 7.83		CPI : 8.00		Total:		1000	742		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : KALURI PRAVEEN RAJA

Semester : II

Mother's Name : ARUNA KUMARI

Roll No : 19266009

Enrollment No : 190803

Father's Name : DHANANJAYA RAO

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	76	30	22	20	14	150	112	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	88	30	27	20	20	150	135	O	10	4.00
ET41213VL	VLSI System Design	100	90	30	28	20	20	150	138	O	10	4.00
ET41235VL	Elective - I (VLSI Technology)	100	91	30	29	20	19	150	139	O	10	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	88	30	27	20	20	150	135	O	10	4.00
ET41221VL	Analog IC Design Lab	50	48			75	72	125	120	O	10	2.00
ET41222VL	System on Programmable chip Design Lab	50	46			75	70	125	116	O	10	2.00
PASS		SPI : 9.66		CPI : 9.41		Total:		1000	895		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : KELLA CHAITANYA

Semester : II

Mother's Name : KELLA LAKSHMI

Roll No : 19266010

Enrollment No : 190017

Father's Name : KELLA THIRUPATHI

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	79	30	25	20	20	150	124	E	09	4.00
ET41212VL	System on Programmable Chip Design	100	90	30	26	20	20	150	136	O	10	4.00
ET41213VL	VLSI System Design	100	89	30	24	20	20	150	133	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	90	30	25	20	20	150	135	O	10	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	87	30	23	20	19	150	129	E	09	4.00
ET41221VL	Analog IC Design Lab	50	40			75	57	125	97	A	08	2.00
ET41222VL	System on Programmable chip Design Lab	50	48			75	70	125	118	O	10	2.00
PASS		SPI : 9.33		CPI : 9.41		Total:		1000	872		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : MINAL BISEN
Mother's Name : LAXMI BISEN
Father's Name : RAMCHAND BISEN

Roll No : 19266011

Semester : II
Enrollment No : 190781

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	80	30	27	20	18	150	125	E	09	4.00
ET41212VL	System on Programmable Chip Design	100	84	30	25	20	20	150	129	E	09	4.00
ET41213VL	VLSI System Design	100	82	30	23	20	20	150	125	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	86	30	27	20	19	150	132	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	81	30	24	20	19	150	124	E	09	4.00
ET41221VL	Analog IC Design Lab	50	48			75	73	125	121	O	10	2.00
ET41222VL	System on Programmable chip Design Lab	50	44			75	68	125	112	E	09	2.00
PASS		SPI : 9.08		CPI : 8.79		Total:		1000	868		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : PRABHAT KUMAR DWIVEDI
Mother's Name : SAVITA DWIVEDI
Father's Name : MAHENDRA KUMAR DWIVEDI

Roll No : 19266013

Semester : II
Enrollment No : 190037

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	75	30	22	20	14	150	111	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	84	30	26	20	20	150	130	E	09	4.00
ET41213VL	VLSI System Design	100	83	30	24	20	18	150	125	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	88	30	29	20	19	150	136	O	10	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	80	30	22	20	19	150	121	E	09	4.00
ET41221VL	Analog IC Design Lab	50	41			75	60	125	101	A	08	2.00
ET41222VL	System on Programmable chip Design Lab	50	40			75	67	125	107	E	09	2.00
PASS		SPI : 8.91		CPI : 8.87		Total:		1000	831		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : PYDI SUNIL KUMAR

Semester : II

Mother's Name : PYDI LAKSHMI

Roll No : 19266014

Enrollment No : 190799

Father's Name : PYDI VENKATA RAMANA

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	81	30	25	20	20	150	126	E	09	4.00
ET41212VL	System on Programmable Chip Design	100	86	30	24	20	20	150	130	E	09	4.00
ET41213VL	VLSI System Design	100	85	30	26	20	20	150	131	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	88	30	26	20	19	150	133	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	81	30	21	20	18	150	120	E	09	4.00
ET41221VL	Analog IC Design Lab	50	40			75	58	125	98	A	08	2.00
ET41222VL	System on Programmable chip Design Lab	50	46			75	70	125	116	O	10	2.00
PASS		SPI : 9.00		CPI : 9.16		Total:		1000	854		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : ROHIT VERMA

Semester : II

Mother's Name : SARITA VERMA

Roll No : 19266015

Enrollment No : 190038

Father's Name : SUSHIL KUMAR VERMA

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	70	30	24	20	12	150	106	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	77	30	21	20	20	150	118	A	08	4.00
ET41213VL	VLSI System Design	100	76	30	19	20	15	150	110	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	81	30	24	20	15	150	120	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	79	30	24	20	19	150	122	E	09	4.00
ET41221VL	Analog IC Design Lab	50	47			75	72	125	119	O	10	2.00
ET41222VL	System on Programmable chip Design Lab	50	40			75	60	125	100	A	08	2.00
PASS		SPI : 8.50		CPI : 8.50		Total:		1000	795		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : SAMIKSHA SHRIVASTAVA

Semester : II

Mother's Name : MAMTA SHRIVASTAVA

Roll No : 19266016

Enrollment No : 190033

Father's Name : ASHWINI KUMAR SHRIVASTAVA

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	71	30	17	20	20	150	108	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	88	30	27	20	20	150	135	O	10	4.00
ET41213VL	VLSI System Design	100	86	30	26	20	20	150	132	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	87	30	24	20	18	150	129	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	84	30	24	20	20	150	128	E	09	4.00
ET41221VL	Analog IC Design Lab	50	34			75	55	125	89	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	44			75	70	125	114	E	09	2.00
PASS		SPI : 8.83		CPI : 8.91		Total:		1000	835		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : SHAIK MUSTHAFA

Semester : II

Mother's Name : SHAIK NOORJAHAN

Roll No : 19266017

Enrollment No : 190779

Father's Name : SHAIK SHAREEF

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	66	30	18	20	18	150	102	B	07	4.00
ET41212VL	System on Programmable Chip Design	100	77	30	23	20	20	150	120	E	09	4.00
ET41213VL	VLSI System Design	100	76	30	22	20	19	150	117	A	08	4.00
ET41235VL	Elective - I (VLSI Technology)	100	79	30	25	20	18	150	122	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	69	30	15	20	16	150	100	B	07	4.00
ET41221VL	Analog IC Design Lab	50	34			75	54	125	88	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	44			75	68	125	112	E	09	2.00
PASS		SPI : 8.00		CPI : 7.91		Total:		1000	761		24.00	



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Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : SHIVANGI GUPTA

Semester : II

Mother's Name : REENA GUPTA

Roll No : 19266019

Enrollment No : 190783

Father's Name : ANIL KUMAR GUPTA

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	69	30	18	20	12	150	99	B	07	4.00
ET41212VL	System on Programmable Chip Design	100	83	30	24	20	20	150	127	E	09	4.00
ET41213VL	VLSI System Design	100	83	30	24	20	16	150	123	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	87	30	24	20	17	150	128	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	77	30	16	20	17	150	110	A	08	4.00
ET41221VL	Analog IC Design Lab	50	31			75	55	125	86	B	07	2.00
ET41222VL	System on Programmable chip Design Lab	50	39			75	67	125	106	E	09	2.00
PASS		SPI : 8.33		CPI : 8.58		Total:		1000	779		24.00	



National Institute of Technology Raipur

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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : SHUBHI KESHERWANI

Semester : II

Mother's Name : NEELU KESHERWANI

Roll No : 19266020

Enrollment No : 190067

Father's Name : SITARAM KESHERWANI

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	75	30	21	20	18	150	114	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	82	30	24	20	20	150	126	E	09	4.00
ET41213VL	VLSI System Design	100	82	30	24	20	19	150	125	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	86	30	25	20	18	150	129	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	83	30	26	20	20	150	129	E	09	4.00
ET41221VL	Analog IC Design Lab	50	41			75	67	125	108	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	46			75	70	125	116	O	10	2.00
PASS		SPI : 8.91		CPI : 8.79		Total:		1000	847		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : VAISHALI SAHU
Mother's Name : SUSHILA SAHU
Father's Name : RAJENDRA KUMAR SAHU

Roll No : 19266021

Semester : II
Enrollment No : 190016

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	78	30	23	20	14	150	115	A	08	4.00
ET41212VL	System on Programmable Chip Design	100	90	30	28	20	20	150	138	O	10	4.00
ET41213VL	VLSI System Design	100	88	30	28	20	20	150	136	O	10	4.00
ET41235VL	Elective - I (VLSI Technology)	100	90	30	27	20	19	150	136	O	10	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	82	30	22	20	19	150	123	E	09	4.00
ET41221VL	Analog IC Design Lab	50	42			75	64	125	106	E	09	2.00
ET41222VL	System on Programmable chip Design Lab	50	46			75	70	125	116	O	10	2.00
PASS		SPI : 9.41		CPI : 9.20		Total:		1000	870		24.00	



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Tabulation Chart : SPRING 2020 (M.Tech.-NIT)

Branch : ELECTRONICS & COMMUNICATION ENGINEERING VLSI DESIGN & EMBEDDED SYSTEM

Name : YETTI RAMYA
Mother's Name : YETTI UMA
Father's Name : YETTI CHALAMAI AH

Roll No : 19266022

Semester : II
Enrollment No : 190023

Subject Code	Subject	E.S.E.		C.T.		T.A.		Total		Grade	GP & Credits	
		MAX	OBT	MAX	OBT	MAX	OBT	MAX	OBT			
ET41211VL	Analog IC Design	100	74	30	30	20	16	150	120	E	09	4.00
ET41212VL	System on Programmable Chip Design	100	78	30	25	20	20	150	123	E	09	4.00
ET41213VL	VLSI System Design	100	78	30	22	20	20	150	120	E	09	4.00
ET41235VL	Elective - I (VLSI Technology)	100	79	30	24	20	18	150	121	E	09	4.00
ET41244VL	Elective - II (Low Power VLSI Design Techniques)	100	70	30	15	20	16	150	101	B	07	4.00
ET41221VL	Analog IC Design Lab	50	38			75	58	125	96	A	08	2.00
ET41222VL	System on Programmable chip Design Lab	50	44			75	70	125	114	E	09	2.00
PASS		SPI : 8.58		CPI : 8.20		Total:		1000	795		24.00	

Appeared	PASS		FAIL				Withheld
Total Student	Number	Percentage	No. of fail students due to Absent	% of fail student due to Absent	Fail + ABS = Total fail in No.	Fail + ABS = Total fail in %	
20	20	100.00	0	0.00	0 + 0 = 0	0.00 + 0.00 = 0.00	0